Arjun Ramesh

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RESEARCH STATEMENT

I specialize in **virtual machines** and **compilers** with an embedded systems flavor. Driven by a bottom-up approach, my research rethinks the software architecture for resource-constrained edge systems around bytecode virtualization to bring modern programmability and deep-stack observability at minimal performance costs.

EDUCATION

Carnegie Mellon University — *PhD+MS, Electrical & Computer Engineering* — *Jun 2026 (Exp.)*
The University of Texas at Austin — *BS, Electrical & Computer Engineering* — *GPA: 4.00 | Aug 2021*

PUBLICATIONS

Empowering WebAssembly with Thin Kernel Interfaces — *1st Author* — *EuroSys '25*
Unveiling Heisenbugs with Diversified Execution — *1st Author* — *Talk* | *OOPSLA '25*
Silverline: Virtualization and Orchestration of Distributed Systems — *1st Author* — *RTAS '25*
Edge Runtime Prediction using Conformal Matrix Completion — *2nd Author* — *MLSys '25*

SELECTED WORK EXPERIENCE

Programmability Intern — *F5 Inc., Office of the CTO (San Jose, CA)* — *Jun-Aug 2025*
Built efficient record/replay feature in Wasmtime compiler to enable time-travel debugging

IoT Cloud and Edge Integration Intern — *Bosch Research (Pittsburgh, PA)* — *Jun-Aug 2022*
Designed an edge-orchestration framework (Silverline) for real-time industrial automation

GPU Design Verification Intern — *Apple Inc. (Austin, TX)* — *Jun-Aug 2020*
Memory hierarchy testing improvements (speed/coverage); UVM testbenches for M2 Graphics

CPU Design Verification Intern — *Centaur Technology Inc. (Austin, TX)* — *May-Aug 2019*
Memory testing tools for x86/AVX-512 chip and live analysis of CPU exception events

SELECTED INVITED TALKS

Time-Travel Debugging for WebAssembly — Wasm Research Day — *Oct '25*
Unveiling CPS Heisenbugs at Scale — Bosch RDS Tech Colloquium — *Oct '24*

SELECTED HONORS

Charles W. and Margaret A. Tolbert Scholarship — High Merit in Engineering — *Fall '20*
Ray Fisher Memorial Scholarship — High Merit University-Wide — *Fall '19*

SELECTED TECHNICAL PROJECTS

RISC-V CPU Design and ISA Extension — *Apr 2021*
Out-of-order RISC-V CPU with custom extensions to accelerate hashsets and graph search — Talk | GH

The JASP Embedded Cellular Phone — *Dec 2019*
Cellphone designed from scratch with call+text; Won popular vote in class project showcase — GH

RTOS Design on Bare-Metal Microcontroller — *Apr 2020*
Fully featured with process loading, priority scheduling, FAT filesystem, and wireless RPCs — Talk